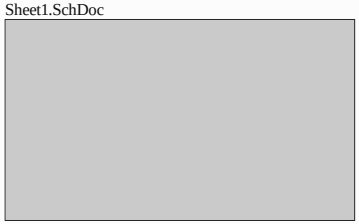
青创电子 QC E-TECH

Cyclone FPGA开发板

Sheet1
Sheet1.SchDoc



Sheet2
Sheet2.SchDoc

Sheet1.sch 最小核心系统

Sheet2.sch 外围设备

Title		
Size A4	Number	Revision
Date: 2014-12-6		Sheet of
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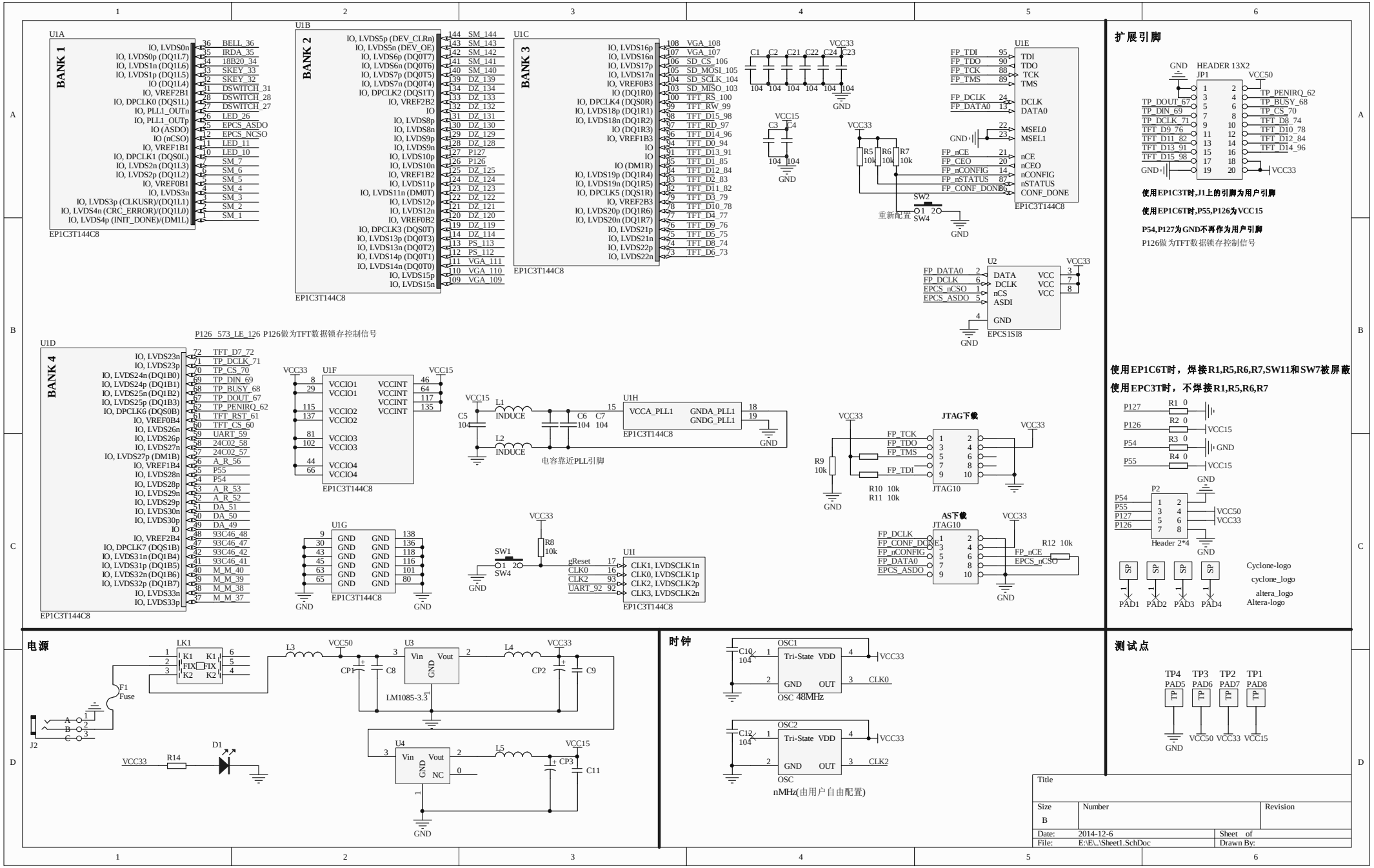
U1A
BANK 1
IO, LVDS0n
IO, LVDS0p (DQ1L7)
IO, LVDS1n (DQ1L6)
IO, LVDS1p (DQ1L5)
IO (DQ1L4)
IO, VREF2B1
IO, DPCLK0 (DQS1L)
IO, PLL1_OUTn
IO, PLL1_OUTp
IO (ASDO)
IO (nCSO)
IO, VREF1B1
IO, DPCLK1 (DQS0L)
IO, LVDS2n (DQ1L3)
IO, LVDS2p (DQ1L2)
IO, VREF0B1
IO, LVDS3n
IO, LVDS3p (CLKUSR)/(DQ1L1)
IO, LVDS4n (CRC_ERROR)/(DQ1L0)
IO, LVDS4p (INIT_DONE)/(DM1L)
BELL_36
IRDA_35
18B20_34
SKEY_33
SKEY_32
DSWITCH_31
DSWITCH_28
DSWITCH_27
LED_26
EPCS_ASDO
EPCS_NCSO
LED_11
LED_10
SM_7
SM_6
SM_5
SM_4
SM_3
SM_2
SM_1
EP1C3T144C8
U1B
BANK 2
IO, LVDS5p (DEV_CLRn)
IO, LVDS5n (DEV_OE)
IO, LVDS6p (DQ0T7)
IO, LVDS6n (DQ0T6)
IO, LVDS7p (DQ0T5)
IO, LVDS7n (DQ0T4)
IO, DPCLK2 (DQS1T)
IO, VREF2B2
IO
IO, LVDS8p
IO, LVDS8n
IO, LVDS9p
IO, LVDS9n
IO, LVDS10p
IO, LVDS10n
IO, VREF1B2
IO, LVDS11p
IO, LVDS11n (DM0T)
IO, LVDS12p
IO, LVDS12n
IO, VREF0B2
IO, DPCLK3 (DQS0T)
IO, LVDS13p (DQ0T3)
IO, LVDS13n (DQ0T2)
IO, LVDS14p (DQ0T1)
IO, LVDS14n (DQ0T0)
IO, LVDS15p
IO, LVDS15n
SM_144
SM_143
SM_142
SM_141
SM_140
DZ_139
DZ_134
DZ_133
DZ_132
DZ_131
DZ_130
DZ_129
DZ_128
P127
P126
DZ_125
DZ_124
DZ_123
DZ_122
DZ_121
DZ_120
DZ_119
DZ_114
PS_113
PS_112
VGA_111
VGA_110
VGA_109
EP1C3T144C8
U1C
BANK 3
IO, LVDS16p
IO, LVDS16n
IO, LVDS17p
IO, LVDS17n
IO, VREF0B3
IO (DQ1R0)
IO, DPCLK4 (DQS0R)
IO, LVDS18p (DQ1R1)
IO, LVDS18n (DQ1R2)
IO (DQ1R3)
IO, VREF1B3
IO
IO
IO (DM1R)
IO, LVDS19p (DQ1R4)
IO, LVDS19n (DQ1R5)
IO, DPCLK5 (DQS1R)
IO, VREF2B3
IO, LVDS20p (DQ1R6)
IO, LVDS20n (DQ1R7)
IO, LVDS21p
IO, LVDS21n
IO, LVDS22p
IO, LVDS22n
VGA_108
VGA_107
SD_CS_106
SD_MOSI_105
SD_SCLK_104
SD_MISO_103
TFT_RS_100
TFT_RW_99
TFT_D15_98
TFT_RD_97
TFT_D14_96
TFT_D0_94
TFT_D13_91
TFT_D1_85
TFT_D12_84
TFT_D2_83
TFT_D11_82
TFT_D3_79
TFT_D10_78
TFT_D4_77
TFT_D9_76
TFT_D5_75
TFT_D8_74
TFT_D6_73
EP1C3T144C8
C1 C2 C21 C22 C24 C23
104 104 104 104 104 104
VCC33
GND
C3 C4
104 104
VCC15
U1E
TDI
TDO
TCK
TMS
DCLK
DATA0
MSEL0
MSEL1
nCE
nCEO
nCONFIG
nSTATUS
CONF_DONE
FP_TDI
FP_TDO
FP_TCK
FP_TMS
FP_DCLK
FP_DATA0
FP_nCE
FP_CEO
FP_nCONFIG
FP_nSTATUS
FP_CONF_DONE
EP1C3T144C8
R5 R6 R7
10k 10k 10k
SW2
SW4
重新配置
U2
DATA
DCLK
nCS
ASDI
GND
VCC
EPCS1SI8
FP_DATA0
FP_DCLK
EPCS_nCSO
EPCS_ASDO
U1D
BANK 4
IO, LVDS23n
IO, LVDS23p
IO, LVDS24n (DQ1B0)
IO, LVDS24p (DQ1B1)
IO, LVDS25n (DQ1B2)
IO, LVDS25p (DQ1B3)
IO, DPCLK6 (DQS0B)
IO, VREF0B4
IO, LVDS26n
IO, LVDS26p
IO, LVDS27n
IO, LVDS27p (DM1B)
IO, VREF1B4
IO, LVDS28n
IO, LVDS28p
IO, LVDS29n
IO, LVDS29p
IO, LVDS30n
IO, LVDS30p
IO
IO, VREF2B4
IO, DPCLK7 (DQS1B)
IO, LVDS31n (DQ1B4)
IO, LVDS31p (DQ1B5)
IO, LVDS32n (DQ1B6)
IO, LVDS32p (DQ1B7)
IO, LVDS33n
IO, LVDS33p
TFT_D7_72
TP_DCLK_71
TP_CS_70
TP_DIN_69
TP_BUSY_68
TP_DOUT_67
TFT_RST_61
TFT_CS_60
UART_59
24C02_58
24C02_57
A_R_56
P55
P54
A_R_53
A_R_52
DA_51
DA_50
DA_49
93C46_48
93C46_47
93C46_42
93C46_41
M_M_40
M_M_39
M_M_38
M_M_37
EP1C3T144C8
P126 573_LE_126 P126做为TFT数据锁存控制信号
U1F
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCINT
VCC15
EP1C3T144C8
U1G
GND
EP1C3T144C8
U1H
VCCA_PLL1
GNDA_PLL1
GNDG_PLL1
L1 INDUCE
L2 INDUCE
C5 104
C6 104
C7 104
电容靠近PLL引脚
EP1C3T144C8
SW1
SW4
R8 10k
gReset
CLK0
CLK2
UART_92
U1I
CLK1, LVDSCLK1n
CLK0, LVDSCLK1p
CLK2, LVDSCLK2p
CLK3, LVDSCLK2n
EP1C3T144C8
JTAG下载
JTAG10
FP_TCK
FP_TDO
FP_TMS
FP_TDI
R9 10k
R10 10k
R11 10k
AS下载
FP_CONF_DONE
FP_nCONFIG
FP_DATA0
EPCS_ASDO
FP_nCE
EPCS_nCSO
R12 10k
扩展引脚
HEADER 13X2
JP1
TP_DOUT_67
TP_DIN_69
TP_DCLK_71
TFT_D9_76
TFT_D11_82
TFT_D13_91
TFT_D15_98
TP_PENIRQ_62
TP_BUSY_68
TP_CS_70
TFT_D8_74
TFT_D10_78
TFT_D12_84
TFT_D14_96
使用EP1C3T时,J1上的引脚为用户引脚
使用EP1C6T时,P55,P126为VCC15
P54,P127为GND不再作为用户引脚
P126做为TFT数据锁存控制信号
使用EP1C6T时，焊接R1,R5,R6,R7,SW11和SW7被屏蔽
使用EPC3T时，不焊接R1,R5,R6,R7
P127 R1 0
P126 R2 0
P54 R3 0
P55 R4 0
P2
Header 2*4
SP
PAD1
PAD2
PAD3
PAD4
Cyclone-logo
cyclone_logo
altera_logo
Altera-logo
电源
LK1
K1
K2
FIX
F1
Fuse
J2
A
B
C
D1
R14
L3
L4
L5
U3
U4
LM1085-3.3
Vin
Vout
GND
NC
CP1
CP2
CP3
C8
C9
C11
时钟
OSC1
OSC2
Tri-State
VDD
OUT
C10 104
C12 104
OSC 48MHz
OSC nMHz(由用户自由配置)
CLK0
CLK2
测试点
TP4 PAD5
TP3 PAD6
TP2 PAD7
TP1 PAD8
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Number
Revision
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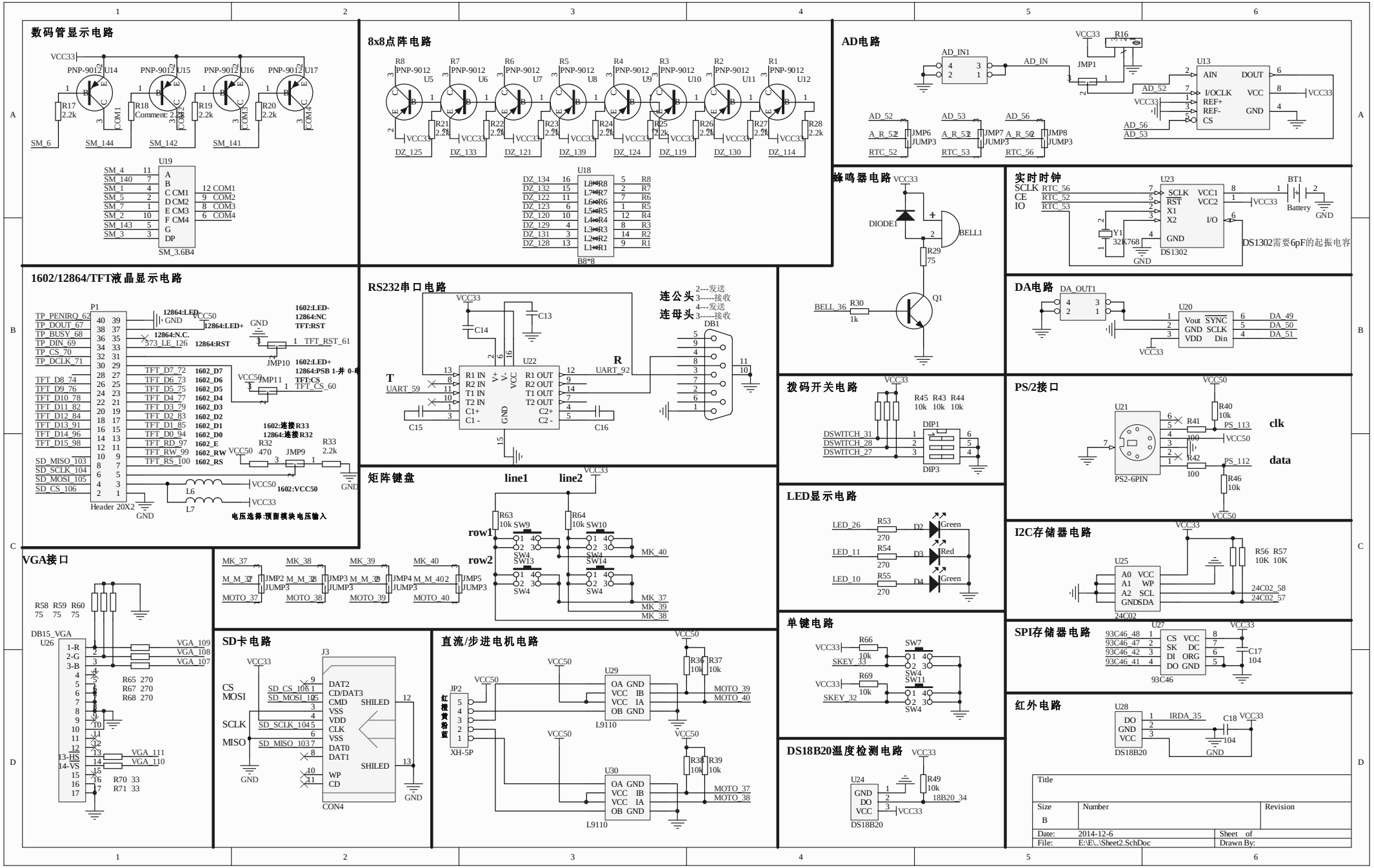
数码管显示电路
8x8点阵电路
AD电路
1602/12864/TFT液晶显示电路
RS232串口电路
蜂鸣器电路
实时时钟
DS1302需要6pF的起振电容
DA电路
拨码开关电路
PS/2接口
clk
data
矩阵键盘
line1
line2
row1
row2
LED显示电路
I2C存储器电路
VGA接口
SD卡电路
直流/步进电机电路
单键电路
SPI存储器电路
DS18B20温度检测电路
红外电路
Title
Size
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